CLAIMS

What is claimed is:

1. A method, comprising:

receiving a legacy type hardware interrupt request ("IRQ") by a processor during a native mode runtime of the processor; and

servicing the legacy type hardware IRQ received during the native mode runtime, wherein the native mode runtime is a higher performance state of the processor than a legacy mode runtime of the processor defined by a number of bits processed in parallel.

2. The method of claim 1, further comprising:

transitioning from the native mode runtime to the legacy mode runtime in response to the legacy type hardware IRQ to service the legacy type hardware IRQ.

3. The method of claim 2 wherein servicing the legacy type hardware IRQ includes:

executing at least one legacy type interrupt service routine ("ISR"); and

returning to the native mode runtime prior to servicing another legacy type hardware IRQ.

4. The method of claim 3 wherein servicing the legacy type hardware IRQ includes servicing the legacy type hardware IRQ with at least one legacy type ISR invoked by a native type ISR.

5. The method of claim 3, further comprising:

copying the at least one legacy type ISR from a firmware unit to system memory; and

servicing the legacy type hardware IRQ with the copied at least one legacy type ISR executed from the system memory.

6. The method of claim 1, further comprising:

receiving a native type hardware IRQ by the processor during the legacy mode runtime of the processor;

transitioning from the legacy mode runtime to the native mode runtime in response to the native type hardware IRQ; and

servicing the native type hardware IRQ.

7. The method of claim 1 wherein the legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

8. The method of claim 1 wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code and 64-bit code and wherein the native mode runtime of the processor includes executing one of 32-bit code and 64-bit code by the processor.

9. The method of claim 1, further comprising:

receiving a legacy type hardware IRQ by the processor during the legacy mode runtime;

transitioning to the native mode runtime in response to the legacy type hardware IRQ to determine a type of the legacy type hardware IRQ;

transitioning back to the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ during the legacy mode runtime of the processor.

10. A machine-accessible medium that provides instructions that, if executed by a machine, will cause the machine to perform operations comprising:

receiving a legacy type hardware interrupt request ("IRQ") by a processor of the machine during a native mode runtime of the processor; and

servicing the legacy type hardware IRQ received during the native mode runtime, wherein the native mode runtime is a higher performance state of the processor than a legacy mode runtime of the processor defined by a number of bits processed in parallel.

11. The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, will cause the machine to perform operations, further comprising:

transitioning from the native mode runtime to the legacy mode runtime in response to the legacy type hardware IRQ to service the legacy type hardware IRQ..

12. The machine-accessible medium of claim 11, further embodying instructions that, if executed by the machine, will cause the machine to perform the operations wherein servicing the legacy type hardware IRQ includes:

executing at least one legacy type interrupt service routine ("ISR"); and

returning to the native mode runtime prior to servicing another legacy type hardware IRQ.

13. The machine-accessible medium of claim 12, further embodying instructions that, if executed by the machine, will cause the machine to perform the operations wherein:

servicing the legacy type hardware IRQ includes servicing the legacy type hardware IRQ with at least one legacy type ISR invoked by a native type ISR.

14. The machine-accessible medium of claim 12, further embodying instructions that, if executed by the machine, will cause the machine to perform operations, further comprising:

copying the at least one legacy type ISR from a firmware unit to system memory; and

servicing the legacy type hardware IRQ with the copied at least one legacy type ISR executed from the system memory.

15. The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform operations, further comprising:

receiving a native type hardware IRQ by the processor during the legacy mode runtime of the processor;

transitioning from the legacy mode runtime to the native mode runtime in response to the native type hardware IRQ; and

servicing the native type hardware IRQ.

16. The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform the operations wherein the legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

17. The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform the operations wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code and 64-bit code and wherein the native mode runtime of the processor includes executing one of 32-bit code and 64-bit code by the processor.

18. The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform operations, further comprising:

receiving a legacy type hardware IRQ by the processor during the legacy mode runtime;

transitioning to the native mode runtime in response to the legacy type hardware IRQ to determine a type of the legacy type hardware IRQ;

transitioning back to the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ during the legacy mode runtime of the processor.

19. A processing system, comprising

a processor to receive a first native type hardware interrupt request ("IRQ") and to receive a first legacy type hardware IRQ during a native mode runtime of the processor; and

a flash memory unit communicatively coupled to the processor and having stored therein at least one legacy type ISR, the processor to execute the at least one legacy type ISR in response to the legacy type hardware IRQ, wherein the native mode runtime is a higher performance state of the processor than a legacy mode runtime of the processor defined by a number of bits processed in parallel.

20. The processing system of claim 19 wherein the processor to transition from the native mode runtime to the legacy mode runtime in response to the legacy type hardware IRQ and prior to executing the at least one legacy type ISR.

21. The processing system of claim 20 wherein the processor to return to the native mode runtime after executing the at least one legacy type ISR and prior to executing another legacy type ISR in response to another legacy type hardware IRQ.

22. The processing system of claim 20 wherein the flash memory unit further having stored therein a native type ISR, the processor to service the first legacy type hardware IRQ by executing the at least one legacy type ISR invoked by the native type ISR.

23. The processing system of claim 19 wherein the processor further to receive a second native type hardware IRQ during the legacy mode runtime of the processor and wherein the flash memory unit further having stored therein at least one native type ISR, the processor to execute the at least one native type ISR in response to the second native type hardware IRQ.

24. The processing system of claim 23 wherein the processor to change from the legacy mode runtime to the native mode runtime in response to the second native type hardware IRQ to execute the at least one native type ISR.

25. The processing system of claim 23, further comprising:

system memory communicatively coupled to the processor and coupled to receive a copy of the at least one native type ISR and a copy of the at least one legacy type ISR from the flash memory unit, the processor to execute the copy of the at least one native type ISR and the copy of the at least one legacy type ISR from the system memory.

26. The processing system of claim 25 wherein the flash memory unit further having stored therein a global interrupt handler, the global interrupt handler to be transferred into system memory, the processor to execute the global interrupt handler in response to either one of the first legacy type hardware IRQ and the first native type hardware IRQ, the global interrupt handler to invoke the copy of the at least one legacy type ISR in response to the first legacy type hardware IRQ and to invoke the copy of the at least one native type ISR in response to the native type hardware IRQ.

27. The processing system of claim 19 wherein first legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

28. The processing system of claim 23 wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code and 64-bit code and wherein the native mode runtime of the processor includes executing one of 32-bit code and 64-bit code by the processor.